I CLAIM:

1. A circuit adapted to generate a tail current for a main amplifier stage, comprising:

a scaled master stage circuit;

a balanced stage circuit;

the scaled master stage circuit responsively coupled to the balanced stage circuit,

the scaled master stage having a predetermined offset operable to force a given tail current to the balanced stage circuit and a main reader amplifier; and

the balanced stage circuit comprising at least one bi-polar and MOS transistor differential pair adapted to provide a balanced offset to the master stage.

2. The circuit of Claim 1, wherein a main amplifier is in combination with the circuit adapted to generate a tail current for the main amplifier stage.

3. The circuit of Claim 1, wherein the bi-polar transistors comprise NPN transistors and the MOS transistors comprise NMOS transistors.

4. The circuit of Claim 1, wherein the bi-polar transistors comprise PNP transistors and the MOS transistors comprise PMOS transistors.

5. The circuit of Claim 1, being adapted to achieve a low, low-corner –3dB frequency and low noise threshold compared to an all bipolar differential pair.

6. The circuit of Claim 1, wherein the tail current of the scaled master stage circuit is adapted to drive semiconductor devices in a reader amplifier.

7. Bias circuitry for a reader amplifier, comprising:

a master transconductance (gm) stage configured as a scaled reader amplifier;

a balanced stage circuit; and

the scaled reader amplifier responsively coupled to the balanced stage circuit.

the scaled reader amplifier operable to provide a tail current for the balanced stage circuit and a reader amplifier.

8. The bias circuitry for a reader amplifier of Claim 7, having an output matching an absolute current as a function of a predetermined voltage input offset.

9. The bias circuitry for a reader amplifier of Claim 8, wherein the predetermined voltage input offset is about 50 mV.

10. The bias circuitry for a reader amplifier of Claim 7, wherein the master transconductance stage has a precise gm independent of processing variations.

11. A circuit arrangement for providing a tail current to an amplifier, comprising:

a scaled master differential stage;

a balanced stage circuit comprising at least one bi-polar and MOS transistor differential pair adapted to provide a balanced offset to the scaled master differential stage;

the scaled master differential stage having a given offset adapted to force a given tail current.

12. The circuit arrangement of Claim 11 in combination with a main reader amplifier.

13. The circuit arrangement of Claim 11, wherein at least one bipolar transistor is responsively coupled to a magneto-resistive element and at least one MOS transistor is responsively coupled to an AC-coupling capacitor.

14. The circuit arrangement of Claim 11 wherein the bipolar transistor comprises an NPN transistor and the MOS transistor comprises an NMOS transistor.

15. The circuit arrangement of Claim 11, wherein the bipolar transistor comprises a PNP transistor and the MOS transistor comprises a PMOS transistor.

16. A tail current generator circuit, comprising:

a master transconductance stage;

a balanced offset stage including at least one bipolar-MOS differential transistor pair adapted to provide a balanced offset to the master transconductance stage;

the master transconductance stage adapted to set a precise transconductance of the bipolar-MOS differential transistor pair; and

the tail current generator circuit responsive to the master transconductance stage and operable to provide an output which matches an absolute current as a function of a predetermined voltage input offset.

17. The tail current generator circuit of Claim 16, wherein the bipolar transistor comprises an NPN transistor and the MOS transistor comprises an NMOS transistor.

18. The tail current generator circuit of Claim 16, wherein the bipolar transistor comprises a PNP transistor and the MOS transistor comprises a PMOS transistor.

19. A method of generating a tail current for an amplifier, comprising the steps of:

adapting a differential, scaled master stage to accept a balanced offset;

generating a current by a feedback arrangement in the differential, scaled master stage;

scaling the current derived in the differential, scaled master stage; and

providing the scaled current as the tail current for an amplifier.

20. The method of generating a tail current of Claim 19, further comprising using a bipolar/MOS differential pair in a balanced stage circuit to provide the balanced offset.

21. The method of generating a tail current in Claim 20, wherein at least one bipolar transistor is responsively coupled to a magneto-resistive element and at least one MOS transistor is responsively coupled to an AC-coupling capacitor.

22. The method of generating a tail current for an amplifier of Claim 19, wherein the differential, scaled master stage is a scaled version of a main reader amplifier input stage.

23. The method of generating a tail current of Claim 19, for use as a bias circuit in a reader amplifier of a disk drive system.